

WHAT IS CLAIMED IS:

1. A simulator apparatus comprising:
 - a simulator model including a functional model for CPU
 - 5 constituting a system to be simulated;
 - a simulator model including a functional model for hardware to be connected to buses linked to the CPU;
 - plural types of interfaces included in the simulator models and enabling plural types of simulators for various
 - 10 uses to access to the functional models; and
 - a simulator controlling device for selecting any of the plural types of the interfaces and accessing the respective functional models via the selected interfaces.
2. A simulator apparatus as claimed in Claim 1, wherein
- 15 the interfaces for the respective functional models comprise an interface usable in a simulator for verifying software.
3. A simulator apparatus as claimed in Claim 1, wherein
- the interfaces for the respective functional models
- 20 comprise an interface usable in a simulator for verifying hardware.
4. A simulator apparatus as claimed in Claim 1, wherein
- the interfaces for the respective functional models
- comprise an interface usable in a simulator for verifying a
- 25 system.
5. A simulator apparatus as claimed in Claim 1, wherein
- the interfaces for the respective functional models
- comprise an interface usable in debugging.
6. A simulator apparatus as claimed in Claim 1, wherein
- 30 an interface capable of simulating clock cycles of the system as precision at processing level is comprised.
7. A simulator apparatus as claimed in Claim 1, wherein
- an interface capable of simulating a simulation time
- for the system as precision at processing level is comprised.

8. A simulator apparatus as claimed in Claim 1, wherein the interfaces for the respective functional models comprise an interface for extension usable in performance analysis.

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